HEWLETT-PACKARD COMPANY
Intellectual Property Administration
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PATENT APPLICATION

ATTORNEY DOCKET NO. 200205355-1

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Scott L. Michaelis et al.

Confirmation No.: 3496

Application No.: 10/606,462

Examiner: J. F. Sugent

Filing Date: June 26, 2003

Group Art Unit: 2116

Title: RESETTING MULTIPLE CELLS WITHIN A PARTITION OF A MULTIPLE PARTITION COMPUTER SYSTEM

Mail Stop Appeal Brief-Patents
Commissioner For Patents
PO Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL OF APPEAL BRIEF

Transmitted herewith is the Appeal Brief in this application with respect to the Notice of Appeal filed on August 2, 2007.

The fee for filing this Appeal Brief is (37 CFR 1.17(c)) $ 0.00

(complete (a) or (b) as applicable)

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136(a) apply.

☐ (a) Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d)) for the total number of months checked below:

☐ 1st Month $120	☐ 2nd Month $450	☐ 3rd Month $1020	☐ 4th Month $1590

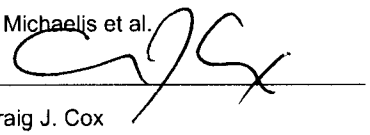
☐ The extension fee has already been filed in this application.

☒ (b) Applicant believes that no extension of time is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

Please charge to Deposit Account 08-2025 the sum of $ 0. At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.16 through 1.21 inclusive, and any other sections in Title 37 of the Code of Federal Regulations that may regulate fees.

Respectfully submitted,

Scott L. Michaelis et al.

By: 

Craig J. Cox

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I hereby certify that this document is being transmitted to the Patent and Trademark Office via eletronic filing.

Date of Transmission: November 9, 2007

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Docket No.: 200205355-1
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Scott L. Michaelis et al.

Application No.: 10/606,462 | Confirmation No.: 3496

Filed: June 26, 2003 | Art Unit: 2116

For: RESETTING MULTIPLE CELLS WITHIN A PARTITION OF A MULTIPLE PARTITION COMPUTER SYSTEM | Examiner: J. F. Sugent

CORRECTED APPEAL BRIEF

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

As required under § 41.37(a), the original brief was filed within two months after the Notice of Appeal filed in this case on August 2, 2007. This Corrected Appeal Brief is filed in response to the Notice of Non-Compliance dated October 12, 2007. Appellant has corrected Section VI. (Grounds of Rejection to be Reviewed on Appeal) and added the requested appendices indicating "none" in each case.

The fees required under § 41.20(b)(2) were paid in the TRANSMITTAL OF APPEAL BRIEF filed with the original brief. Applicant believes no additional fees are due with this Corrected Appeal Brief.

This brief contains items under the following headings as required by 37 C.F.R. § 41.37 and M.P.E.P. § 1205.2:

I. REAL PARTY IN INTEREST

The real party in interest for this appeal is:

Hewlett-Packard Development Company, L.P., a Limited Partnership established under the laws of the State of Texas and having a principal place of business at 20555 S.H. 249, Houston, TX 77070, U.S.A. (hereinafter "HPDC"). HPDC is a Texas limited partnership and is a wholly-owned affiliate of Hewlett-Packard Company, a Delaware Corporation, headquartered in Palo Alto, CA. The general or managing partner of HPDC is HPQ Holdings, LLC.

II. RELATED APPEALS AND INTERFERENCES

There are no other appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

A. Total Number of Claims in Application

There are 23 claims pending in application.

B. Current Status of Claims

1. Claims canceled: None

2. Claims withdrawn from consideration but not canceled: None

3. Claims pending: 1-23

4. Claims allowed: None

5. Claims rejected: 1-3, 5-7, 9-10, and 12-23

6. Claims objected to as dependent on a rejected base claim but otherwise allowable: 4, 8, and 11

C. Claims On Appeal

The claims on appeal are claims 1-3, 5-7, 9-10, and 12-23

IV. STATUS OF AMENDMENTS

Appellant did not file an Amendment After Final Rejection.

V. SUMMARY OF CLAIMED SUBJECT MATTER

According to claim 1, a method for resetting a partition of a multiple partition system is described wherein the partition comprises a plurality of processors. The method includes executing (page 3, line 1), by one processor of the plurality of processors (412, Figure 4; page 3, line 1), a reset code from firmware (410, Figure 4; page 3, line 1) and building a list of reset register addresses associated with the plurality of processors (413, 416, Figure 4; page 6, lines 10-11). The method further includes sending an interrupt (page 6, line 24) to the other processors of the plurality of processors (414, 415, Figure 4; page 6, line 24), resetting the other processors by writing a reset code to their associated reset registers (page 7, lines 24-28), and resetting the one processor by writing to its associated reset register (page 7, lines 29-30).

According to claim 15, a partition of multiple partition computer system is described. The partition includes a plurality of processors (302, Figure 3; page 4, line 12), firmware comprising a reset code (410, Figure 4; page 5, line 14) that resets a portion of the partition (page 6, lines 24-26), wherein one processor of the plurality of processors executes the reset code (412, Figure 4; page 6, lines 22-23) and random access memory that is not affected by the reset code, that stores a list of addresses associated with the portion (page 6, lines 13-14).

According to claim 17, the partition of claim 15, further comprising a plurality of cells (200, Figure 2); wherein each cell comprises at least one processor of the plurality of processors (202, Figure 2), and each cell comprises a reset register having an address that is on the list (413, 416, Figure 4; page 6, lines 10-14). According to claim 20, the partition of claim 17, wherein each cell further comprises resources other than the at least one processor, and a portion of the resources is reset when the cell is reset (page 3, lines 17-19).

According to claim 23, a computer readable medium having computer program logic recorded thereon for operating a partition of a multiple partition computer system (203, 204, Figure 2) is described, wherein the partition includes a plurality of processors (202, Figure 2) The computer program logic includes means for building a list of reset register addresses associated with the plurality of processors (507, Figure 5; page 6, lines 10-11), means for placing each processor of the plurality of processors into a known state (page 3, lines 24-25), and means for resetting the plurality of processors by writing a reset code into their associated reset registers (page 7, lines 24-26).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. First Ground of Rejection

Claims 15-20 and 23 are rejected under 35 U.S.C. § 102(b) as being anticipated by Walton et al. (U.S. Patent No. 7, 103,639) (hereinafter Walton).

B. Second Ground of Rejection

Claims 1-3, 5-7, 9-10, and 12-13 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Walton in view of Harrington et al. (U.S. Patent Publication No2003/0236972 A1) (hereinafter Harrington).

C. Third Ground of Rejection

Claims 14 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Walton and Harrington as applied to claim 1 above, and further in view of Appellant's Admitted Prior art (hereinafter AAPA).

D. Fourth Ground of Rejection

Claims 21 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Walton as applied to claim 1 above, and further in view of Harrington.

E. Fifth Ground of Rejection

Claims 22 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Walton as applied to claim 15 above, and further in view of AAPA.

VII. ARGUMENT

A. First Ground of Rejection

Claims 15-20 and 23 are rejected under 35 U.S.C. § 102(b) as being anticipated by Walton.

It is well settled that to anticipate a claim, the reference must teach every element of the claim. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987). Moreover, in order for a prior art reference to be anticipatory under 35 U.S.C. § 102 with respect to a claim, "[t]he elements must be arranged as required by the claim." *In re Bond*, 15 U.S.P.Q.2d 1566 (Fed. Cir. 1990). Furthermore, in order for a prior art reference to be anticipatory under 35 U.S.C. § 102 with respect to a claim, "[t]he identical invention must be shown in as complete detail as is contained in the . . . claim," *Richardson v. Suzuki Motor Co.*, 9 U.S.P.Q.2d 1913 (Fed. Cir. 1989). Appellants respectfully assert that the rejection does not satisfy these requirements.

Claims 15-19

Claim 15 requires, in part, firmware comprising a reset code that resets a portion of the partition, wherein one processor of the plurality of processors executes the reset code, and random access memory that is not affected by the reset code, that stores a list of addresses associated with the portion. Walton does not describe at least these limitations.

Walton describes a system for managing the formation of a partition from a plurality of independent cells. Abstract. Specifically, Walton describes configuration activities that occur to transition from having individual cells acting independently, to having cells rendezvous and become interdependent to continue operations as a partition. Abstract.

Individual cells may be reset during the partition formation process if they contain the wrong configuration or cached values, or if the cells are not compatible with the partition or otherwise malfunction. Column 6, lines 47-52.

The resetting of cells described by Walton occurs before the inclusion of that cell in a partition. Walton, therefore does not ever describe the resetting of the partition or a portion of the partition as required by claims 15-20 as the reset cells were never part of a partition that could be reset. The Appellee asserts that the monarch processor of Walton includes booting code which is inclusive of initialization and reset, citing column 3, lines 5-12 and column 5, lines 35-47. Appellant respectfully disagrees with the Appellee's characterization of the cited portions of Walton.

Column 3, lines 5-12 define a cell as including a processor dependent hardware (PDH) module which implements instructions executed on CPUs 302 pertaining to the formation of partitions. No mention is made of resetting a portion of a partition after it has been formed. Column 5, lines 35-47 describes a portion of Figure 2 which relates to "the partition formation process". Column 5, lines 35-36. The cited portion states that one processor of CPUs 302 is arbitrarily selected to manage the booting and partition formation activities associated with its respective cell. Column 5, lines 43-45. Again no mention is made of code for resetting a portion of a partition as required by claim 15.

While Walton is very detailed in its description of the partition formation process, Appellant can find no description in Walton of resetting a partition or portion of a partition as required in the rejected claims. Walton describes resetting individual cells that are rejected as part of the partition formation process (see, Figure 2), but that is not the same as a partition reset.

Claim 15 also requires random access memory that is not affected by the reset code, that stores a list of addresses associated with the portion. The Appellee also states that cell micro-controllers (CMs) 304 in each cell as meeting this limitation. The Appellee points to the complex configuration stored in each CM as meeting necessarily including a list of addresses and cites to column 4, line 64 through column 5, line 22 in support of this position. Appellant respectfully disagrees with the Appellee's characterization. Appellant can find no

description in Walton of the CM that refers to a list of addresses for a portion of a partition being reset that is stored in the complex characterization of the CM. The closest reference in the portion of Walton cited by the Appellee is column 5, lines 5 and 6 which recite that the "complex profile essentially provides a map or set of instructions defining the partition scheme of complex 108." Again, no mention is made in Walton, including in the Appellee's cited description, of random access memory that is not affected by the reset code, that stores a list of addresses associated with the portion. Even if each complex characterization stored a list of all the cells in a partition, this is not equivalent to a list of addresses associated with a portion of a partition being reset as required by claim 15.

On page 9 of the Final Office Action dated May 3, 2007 (the "Final Office Action"), the Appellee, in response to Appellant's arguments, again states that Walton teaches "a portion of a partition (cell) being reset (step 206) by a monarch processor (column 6, lines 49-57)," and states that Appellant agrees with Appellee's arguments. Appellant respectfully disagrees with both the Appellee's characterization of Walton and of Appellant's arguments in the Amendment dated February 13, 2007 (the "Amendment").

Appellee's argument ignores the description in Walton that the cell being reset in Walton is not yet part of the partition. Column 6, lines 51-54 of Walton clearly states that the resetting of the cell "does not necessarily prevent the cell from joining the partition." As Walton explicitly states that the cell being reset has not yet joined a partition, the resetting of that cell cannot be resetting a portion of a partition as required by claim 15. In ignoring this aspect of Walton, Appellee also mischaracterizes Appellant's arguments and ignores the distinction that Appellant makes between the present claims and Walton.

As claim 15, and claims 16-19 through their dependency from claim 15, include limitations as described above that are not found in Walton. Claims 15-20 are, therefore, allowable over the rejection of record.

Claim 20

Claim 20, depending from claim 17, requires each cell to further comprise resources other than the at least one processor, where a portion of the resources is reset when a cell is reset. The Appellee rejects claim 20 by stating that it is directed to the partition steps set

forth in claim 17 and offers no additional support for the rejection. Appellant respectfully submits that claim 20 includes limitations not found in claim 17. Specifically, claim 17 does not describe resetting resources other than the at least one processor when the cell is reset. Appellant further respectfully submits that Walton does not describe this limitation and the Appellee has provided no reference to Walton showing this limitation. Appellant, therefore, respectfully submits that claim 20 is allowable over the rejection of record.

Claim 23

Claim 23 requires means for building a list of reset register addresses associated with the plurality of processors, means for placing each processor of the plurality of processors into a known state, and means for resetting the plurality of processors by writing a reset code into their associated reset registers.

As described with respect to claim 15, Walton describes a partition formation process and mechanism, but does not disclose anything related to a means for resetting a plurality of processors by writing a reset code into their associated reset registers. The Appellee has referenced the BIB code described by Walton as meeting the limitation of a reset code. Appellant respectfully disagrees. The BIB, or boot inhibit bit, causes the boot process of a processor or cell to continue to a particular point. Column 4, lines 51-56. The boot inhibit bit may be used to enter a spin loop cycle until the boot inhibit bit is released by the service processor. Column 6, lines 7-11. As described by Walton, including those portion of Walton cited by the Appellee, the boot inhibit bit stops the boot process at specific states to allow for the rendezvous of cells in the partition formation process. The boot inhibit bit is not a reset code as required by claim 23.

The Appellee responds in the Final Office Action by asserting that "in order to reset a processor, a reset code (bit) is inherently written to the reset register of the processor to reset the processor." Final Office Action, Page 10. However, Appellee provides no support for this contention in Walton, nor in any other reference of record. As the rejection of record for claim 23 is under 35 U.S.C. § 102, the "identical invention must be shown in as complete detail as is contained in the . . . claim," *Richardson v. Suzuki Motor Co.*, 9 U.S.P.Q.2d 1913 (Fed. Cir. 1989).

As Walton does not describe means for building a list of reset registers, or means for resetting the plurality of processors by writing a reset code, Walton does not describe each and every limitation of claim 23 as is required by 35 U.S.C. § 102, Appellant asserts that claim 23 is allowable over the rejection of record.

B. Second Ground of Rejection

Claims 1-13 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Walton in view of Harrington. While the rejection on page 4 of the Final Office Action states that claims 1-13 are rejected, Appellee on page 9 of the Final Office Action states that claims 4, 8 and 11 would be allowable if rewritten in independent form. Appellee will proceed on this basis.

To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure, *In re Vaeck* (MPEP 2142). Appellant asserts that at least the first and third criteria have not been met.

Lack of All Claim Limitations.

Claims 1-3, 5-7, 9-10 and 12

Claim 1 requires executing, by one processor of the plurality of processors, a reset code from firmware, building a list of reset register addresses associated with the plurality of processors, sending an interrupt to the other processors of the plurality of processors, resetting the other processors by writing a reset code to their associated reset registers, and resetting the one processor by writing to its associated reset register. The combination put forth by the Appellee does not describe these limitations.

The Appellee asserts that Walton booting code which is inclusive of initialization and reset (Office Action, page 4) citing the firmware code described at column 3, lines 5-12 and column 5, lines 35-47, and a list of reset register addresses citing to the complex profile described at column 2, lines 7-15 and column 4, line 47 through column 5, line 34. Harrington is not relied upon as describing these limitations. Appellant again respectfully disagrees with the Appellee's characterization of Walton.

As set forth with reference to claims 15 and 23, Walton describes a method and mechanism for forming partitions from multiple independent cells. Abstract. Walton, however is completely silent to resetting partitions or portions of partitions using a reset code from firmware. The only description of resetting is the resetting of individual cells and then only as part of a partition formation process when an individual cell does not meet criteria of the formation process. See, Figure 2. Walton does not describe resetting partitions as the cell being reset has not yet completed the partition formation process. Column 6, lines 49-57.

Further, the description of the complex profile does not include a description of a list of reset register addresses associated with the plurality of processors. Appellant has requested that if Appellee is aware of details of the Walton device beyond that described in Walton, that the information be made of record and supplied to the Appellant. Appellee has made no such information of record.

Claims 2, 3, 5-7, 9-10, and 12 depend directly from claim 1 and inherit all the limitations thereof. As Walton does not describe, and Harrington is not relied upon as describing, the limitations set forth above, Appellant respectfully asserts that claims 1-3, 5-7, 9-10, and 12 are allowable over the rejection of record.

Lack of Motivation

The mere fact that references can be combined does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. see In re Mills, 916 F.2d 680 (Fed. Cir. 1990). Appellant respectfully submits that neither Walton, nor Harrington provides motivation for the combination, as the Appellee suggests.

The Appellee's stated motivation for combining Harrington with Walton is "as doing so would give the added benefit of having a more reliable reboot process in a partition system ensuring all pending I/O requests within the system are halted/completed (as taught by Harrington above). As described by Appellant, Walton is completely silent as to resetting partitions or portions of partitions. As Walton is drawn to partition formation and not resetting and contains no description of partition resetting there is no motivation to combine Walton with Harrington to give Walton a "more reliable reboot process in a partition system" as asserted by the Appellee.

Appellee argues in the Final Office Action at page 11 that the motivation is proper as it was taken directly from the secondary reference. Appellant again respectfully asserts that as Walton is silent to partition rebooting, the motivation cited by the Appellee is not relevant to the teachings of Walton and is therefore improper.

Appellant would respectfully assert that the suggestion to make the claimed combination and reasonable expectation of success must both be found in the prior art and not based on the Appellant's disclosure. In re Vaeck, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991). For the reasons set forth above Appellant respectfully asserts that there is no motivation to combine Harrington and Walton. Appellant, therefore, respectfully requests that the rejections based on the combination of Harrington and Walton be withdrawn.

C. Third Ground of Rejection

Claims 14 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Walton and Harrington as applied to claim 1 above, and further in view of AAPA.

Claim 14 depends from claim 1 and therefore inherit all the limitations thereof. Further Applicant respectfully traverses the combination of Walton and Harrington on the grounds set forth above. Claim 14, therefore, is allowable for at least the reasons set forth above with respect to claim 1 and the lack of motivation arguments set forth above.

D. Fourth Ground of Rejection

Claims 21 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Walton as applied to claim 1 above, and further in view of Harrington.

Claim 21 depends from claim 15 and therefore inherit all the limitations thereof. Further Applicant respectfully traverses the combination of Walton and Harrington on the grounds set forth above. Claim 21, therefore, is allowable for at least the reasons set forth above with respect to claim 15 and the lack of motivation arguments set forth above.

E. Fifth Ground of Rejection

Claims 22 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Walton as applied to claim 15 above, and further in view of AAPA.

Claim 22 depends from claim 15 and therefore inherit all the limitations thereof. Further Applicant respectfully traverses the combination of Walton and Harrington on the grounds set forth above. Claim 22, therefore, is allowable for at least the reasons set forth above with respect to claim 15 and the lack of motivation arguments set forth above.

APPENDIX A: CLAIMS

A copy of the claims involved in the present appeal is attached hereto as Appendix A. As indicated above, the claims in Appendix A include the amendments filed by Appellant on May 3, 2007.

APPENDIX B: EVIDENCE APPENDIX

No evidence pursuant to §§ 1.130, 1.131, or 1.132 or entered by or relied upon by the examiner is being submitted.

APPENDIX C: RELATED PROCEEDINGS APPENDIX

No related proceedings are referenced in II. above, hence copies of decisions in related proceedings are not provided.

Appellant believes no additional fee is due with this response. However, if an additional fee is due, please charge Deposit Account No. 08-2025, under Order No. 200205355-1 from which the undersigned is authorized to draw.

Dated: November 9, 2007

Respectfully submitted,

By _____
Craig J. Cox
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I hereby certify that this document is being transmitted to the US Patent and Trademark Office via electronic filing.

Date of Electronic Filing: November 9, 2007
Signature: _____
(Jan Cleveland)

APPENDIX A

Claims Involved in the Appeal of Application Serial No. 10/606,462

1. A method for resetting a partition of a multiple partition system, wherein the partition comprises a plurality of processors, the method comprising:

executing, by one processor of the plurality of processors, a reset code from firmware;

building a list of reset register addresses associated with the plurality of processors;

sending an interrupt to the other processors of the plurality of processors;

resetting the other processors by writing a reset code to their associated reset registers; and

resetting the one processor by writing to its associated reset register.

2. The method of claim 1, further comprising:

storing the firmware on a read only memory.

3. The method of claim 1, further comprising:

storing the list of reset register addresses in random access memory.

4. The method of claim 1, wherein the last reset register address on the list is a reset register address for the cell that is executing the reset code.

5. The method of claim 1, further comprising:

requesting the execution of the reset code by a processor of the plurality of processors.

6. The method of claim 1, further comprising:

requesting the execution of the reset code by an operating system of the multiple partition system.

7. The method of claim 1, further comprising:

requesting the execution of the reset code by a firmware shell of the multiple partition system.

8. The method of claim 1, wherein building the list comprises:

writing the address of the one processor last in the list.

9. The method of claim 1, further comprising:

flushing a cache associated with the one processor, after sending the interrupt.

10. The method of claim 1, further comprising:

moving execution from main memory to read only memory.

11. The method of claim 1, further comprising:

switching from virtual memory mode into physical memory mode.

12. The method of claim 1, wherein the partition comprises a plurality of cells, and each cell comprises at least one processor, the method further comprises:

inventorying the plurality of cells for resetting.

13. The method of claim 1, wherein resetting the one processor occurs after resetting the other processors.

14. The method of claim 1, wherein the plurality of processors are IA-64 processors, and the firmware is system abstraction layer firmware.

15. A partition of multiple partition computer system comprising:

a plurality of processors;

firmware comprising a reset code that resets a portion of the partition, wherein one processor of the plurality of processors executes the reset code; and

random access memory that is not affected by the reset code, that stores a list of addresses associated with the portion.

16. The partition of claim 15, further comprising:

read only memory that stores the firmware.

17. The partition of claim 15, further comprising:

a plurality of cells;

wherein each cell comprises at least one processor of the plurality of processors, and each cell comprises a reset register having an address that is on the list.

18. The partition of claim 17, wherein each cell is reset by writing a reset code to its associated reset register.

19. The partition of claim 17, wherein the address on the list is a reset register address for the cell that comprises the one processor.

20. The partition of claim 17, wherein each cell further comprises resources other than the at least one processor, and a portion of the resources is reset when the cell is reset.

21. The partition of claim 15, wherein the one processor is reset after the other processors of the plurality of processors are reset.

22. The partition of claim 15, wherein the plurality of processors are IA-64 processors, and the firmware is system abstraction layer firmware.

23. A computer readable medium having computer program logic recorded thereon for operating a partition of a multiple partition computer system, wherein the partition comprises a plurality of processors, the computer program logic comprising:

means for building a list of reset register addresses associated with the plurality of processors;

means for placing each processor of the plurality of processors into a known state; and

means for resetting the plurality of processors by writing a reset code into their associated reset registers.

APPENDIX B

Evidence Appendix

No evidence pursuant to §§ 1.130, 1.131, or 1.132 or entered by or relied upon by the examiner is being submitted.

APPENDIX C

Related Proceedings Appendix

No related proceedings are referenced in II. above, hence copies of decisions in related proceedings are not provided.